

L293, L293D QUADRUPLE HALF-H DRIVERS

SLRS008C – SEPTEMBER 1986 – REVISED NOVEMBER 2004

- **Featuring Unitrode L293 and L293D Products Now From Texas Instruments**
- **Wide Supply-Voltage Range: 4.5 V to 36 V**
- **Separate Input-Logic Supply**
- **Internal ESD Protection**
- **Thermal Shutdown**
- **High-Noise-Immunity Inputs**
- **Functionally Similar to SGS L293 and SGS L293D**
- **Output Current 1 A Per Channel (600 mA for L293D)**
- **Peak Output Current 2 A Per Channel (1.2 A for L293D)**
- **Output Clamp Diodes for Inductive Transient Suppression (L293D)**

description/ordering information

The L293 and L293D are quadruple high-current half-H drivers. The L293 is designed to provide bidirectional drive currents of up to 1 A at voltages from 4.5 V to 36 V. The L293D is designed to provide bidirectional drive currents of up to 600-mA at voltages from 4.5 V to 36 V. Both devices are designed to drive inductive loads such as relays, solenoids, dc and bipolar stepping motors, as well as other high-current/high-voltage loads in positive-supply applications.

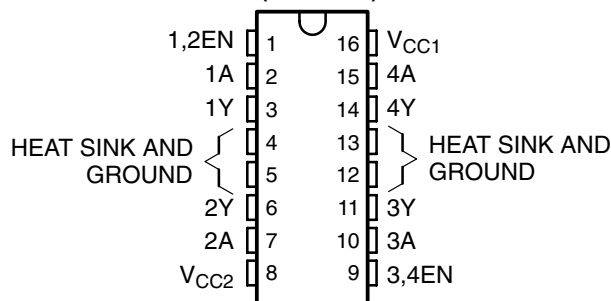
All inputs are TTL compatible. Each output is a complete totem-pole drive circuit, with a Darlington transistor sink and a pseudo-Darlington source. Drivers are enabled in pairs, with drivers 1 and 2 enabled by 1,2EN and drivers 3 and 4 enabled by 3,4EN. When an enable input is high, the associated drivers are enabled, and their outputs are active and in phase with their inputs. When the enable input is low, those drivers are disabled, and their outputs are off and in the high-impedance state. With the proper data inputs, each pair of drivers forms a full-H (or bridge) reversible drive suitable for solenoid or motor applications.

ORDERING INFORMATION

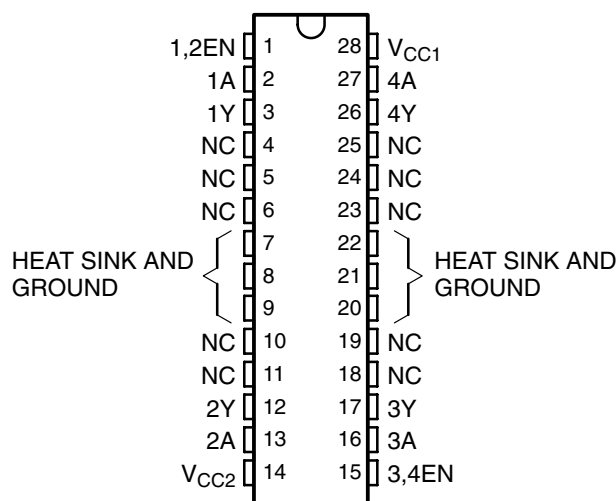
| T _A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------|------------|-----------------------|------------------|
| 0°C to 70°C | HSOP (DWP) | Tube of 20 | L293DWP | L293DWP |
| | PDIP (N) | Tube of 25 | L293N | L293N |
| | PDIP (NE) | Tube of 25 | L293NE | L293NE |
| | | Tube of 25 | L293DNE | L293DNE |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

L293 . . . N OR NE PACKAGE
L293D . . . NE PACKAGE
(TOP VIEW)



L293 . . . DWP PACKAGE
(TOP VIEW)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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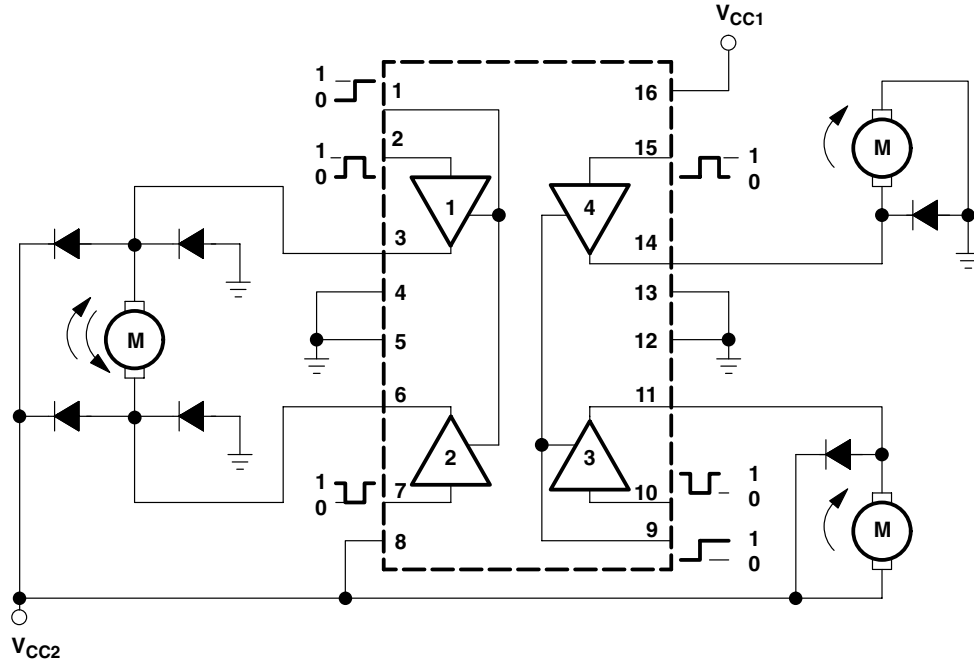
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description/ordering information (continued)

On the L293, external high-speed output clamp diodes should be used for inductive transient suppression. A V_{CC1} terminal, separate from V_{CC2} , is provided for the logic inputs to minimize device power dissipation. The L293 and L293D are characterized for operation from 0°C to 70°C.

block diagram



NOTE: Output diodes are internal in L293D.

FUNCTION TABLE
(each driver)

| INPUTS† | | OUTPUT |
|---------|----|--------|
| A | EN | Y |
| H | H | H |
| L | H | L |
| X | L | Z |

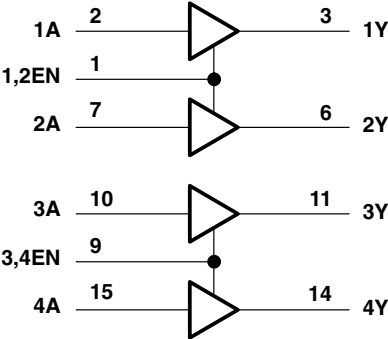
H = high level, L = low level, X = irrelevant, Z = high impedance (off)

† In the thermal shutdown mode, the output is in the high-impedance state, regardless of the input levels.

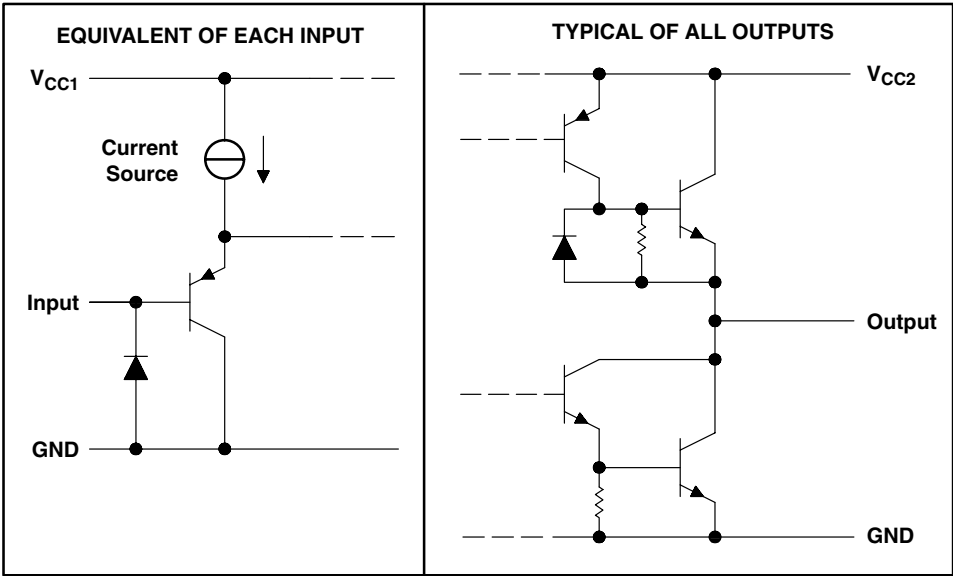
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logic diagram



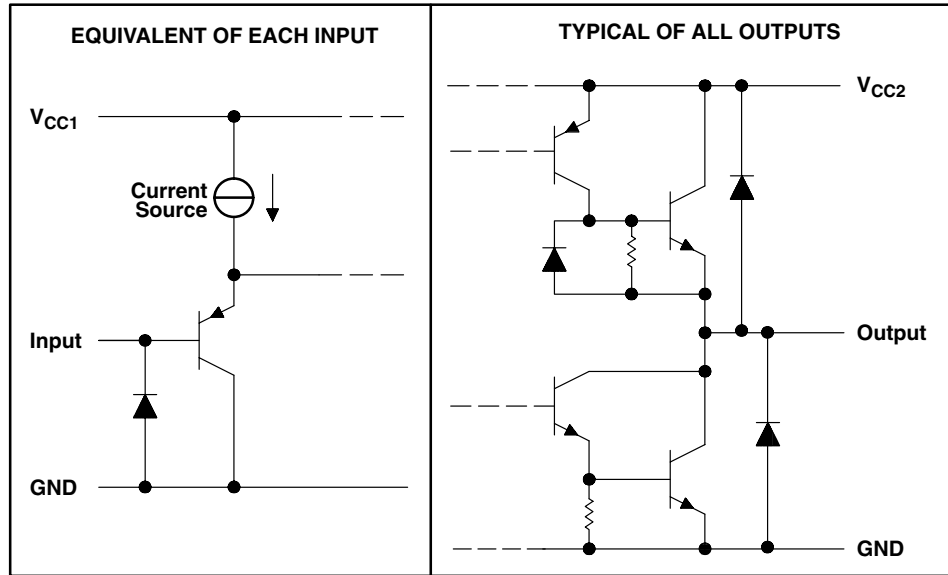
schematics of inputs and outputs (L293)



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schematics of inputs and outputs (L293D)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|---------------------------------------------------------------------------|--------------------------------------|
| Supply voltage, V_{CC1} (see Note 1) | 36 V |
| Output supply voltage, V_{CC2} | 36 V |
| Input voltage, V_I | 7 V |
| Output voltage range, V_O | -3 V to $V_{CC2} + 3$ V |
| Peak output current, I_O (nonrepetitive, $t \leq 5$ ms): L293 | ± 2 A |
| Peak output current, I_O (nonrepetitive, $t \leq 100$ μ s): L293D | ± 1.2 A |
| Continuous output current, I_O : L293 | ± 1 A |
| Continuous output current, I_O : L293D | ± 600 mA |
| Package thermal impedance, θ_{JA} (see Notes 2 and 3): DWP package | TBD $^{\circ}$ C/W |
| N package | 67 $^{\circ}$ C/W |
| NE package | TBD $^{\circ}$ C/W |
| Maximum junction temperature, T_J | 150 $^{\circ}$ C |
| Storage temperature range, T_{stg} | -65 $^{\circ}$ C to 150 $^{\circ}$ C |

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values are with respect to the network ground terminal.
 2. Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150 $^{\circ}$ C can affect reliability.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions

| | | MIN | MAX | UNIT |
|--------------------------------------|---------------------------|-----------|-----------|------|
| Supply voltage | V_{CC1} | 4.5 | 7 | V |
| | V_{CC2} | V_{CC1} | 36 | |
| V_{IH} High-level input voltage | $V_{CC1} \leq 7\text{ V}$ | 2.3 | V_{CC1} | V |
| | $V_{CC1} \geq 7\text{ V}$ | 2.3 | 7 | V |
| V_{IL} Low-level output voltage | | -0.3† | 1.5 | V |
| T_A Operating free-air temperature | | 0 | 70 | °C |

† The algebraic convention, in which the least positive (most negative) designated minimum, is used in this data sheet for logic voltage levels.

electrical characteristics, $V_{CC1} = 5\text{ V}$, $V_{CC2} = 24\text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-------------------------------------------|----|-----------------------------------------------------------------|-------------------------------|-----------------|-----------------|------|---------------|
| V_{OH} High-level output voltage | | L293: $I_{OH} = -1\text{ A}$ L293D: $I_{OH} = -0.6\text{ A}$ | | $V_{CC2} - 1.8$ | $V_{CC2} - 1.4$ | | V |
| V_{OL} Low-level output voltage | | L293: $I_{OL} = 1\text{ A}$ L293D: $I_{OL} = 0.6\text{ A}$ | | | 1.2 | 1.8 | V |
| V_{OKH} High-level output clamp voltage | | L293D: $I_{OK} = -0.6\text{ A}$ | | | $V_{CC2} + 1.3$ | | V |
| V_{OKL} Low-level output clamp voltage | | L293D: $I_{OK} = 0.6\text{ A}$ | | | 1.3 | | V |
| I_{IH} High-level input current | A | $V_I = 7\text{ V}$ | | | 0.2 | 100 | μA |
| | EN | | | | 0.2 | 10 | |
| I_{IL} Low-level input current | A | $V_I = 0$ | | | -3 | -10 | μA |
| | EN | | | | -2 | -100 | |
| I_{CC1} Logic supply current | | $I_O = 0$ | All outputs at high level | | 13 | 22 | mA |
| | | | All outputs at low level | | 35 | 60 | |
| | | | All outputs at high impedance | | 8 | 24 | |
| I_{CC2} Output supply current | | $I_O = 0$ | All outputs at high level | | 14 | 24 | mA |
| | | | All outputs at low level | | 2 | 6 | |
| | | | All outputs at high impedance | | 2 | 4 | |

switching characteristics, $V_{CC1} = 5\text{ V}$, $V_{CC2} = 24\text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | L293NE, L293DNE | | | UNIT |
|-------------------------------------------------------------------------|--|-------------------------------------|-----------------|-----|-----|------|
| | | | MIN | TYP | MAX | |
| t_{PLH} Propagation delay time, low-to-high-level output from A input | | $C_L = 30\text{ pF}$, See Figure 1 | | 800 | | ns |
| t_{PHL} Propagation delay time, high-to-low-level output from A input | | | | 400 | | ns |
| t_{TLH} Transition time, low-to-high-level output | | | | 300 | | ns |
| t_{THL} Transition time, high-to-low-level output | | | | 300 | | ns |

switching characteristics, $V_{CC1} = 5\text{ V}$, $V_{CC2} = 24\text{ V}$, $T_A = 25^\circ\text{C}$

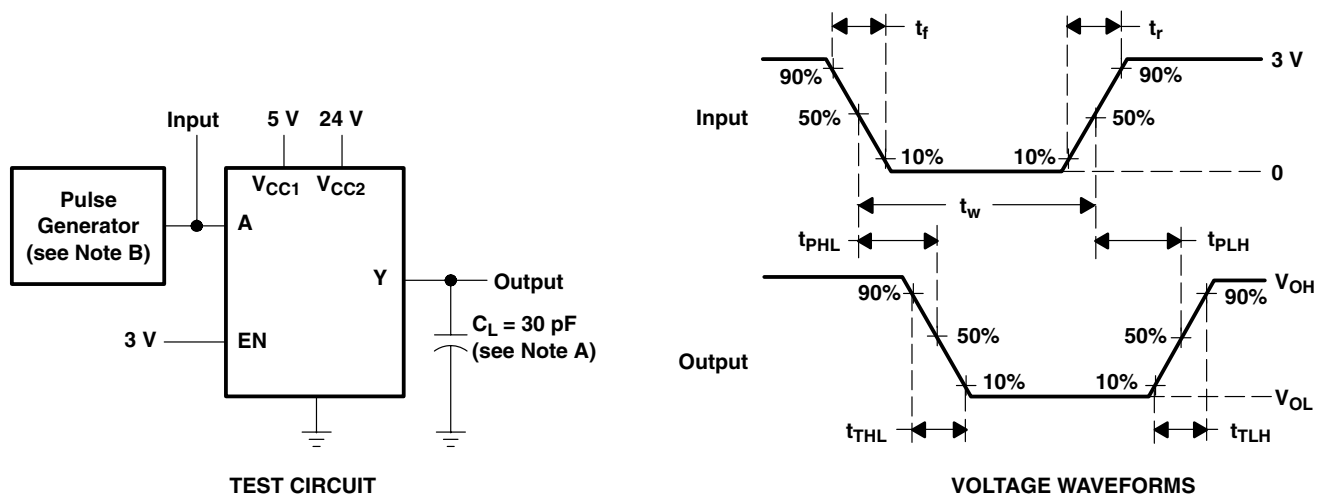
| PARAMETER | | TEST CONDITIONS | L293DWP, L293N L293DN | | | UNIT |
|-------------------------------------------------------------------------|--|-------------------------------------|--------------------------|-----|-----|------|
| | | | MIN | TYP | MAX | |
| t_{PLH} Propagation delay time, low-to-high-level output from A input | | $C_L = 30\text{ pF}$, See Figure 1 | | 750 | | ns |
| t_{PHL} Propagation delay time, high-to-low-level output from A input | | | | 200 | | ns |
| t_{TLH} Transition time, low-to-high-level output | | | | 100 | | ns |
| t_{THL} Transition time, high-to-low-level output | | | | 350 | | ns |



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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 10$ μ s, PRR = 5 kHz, $Z_O = 50$ Ω .

Figure 1. Test Circuit and Voltage Waveforms

APPLICATION INFORMATION

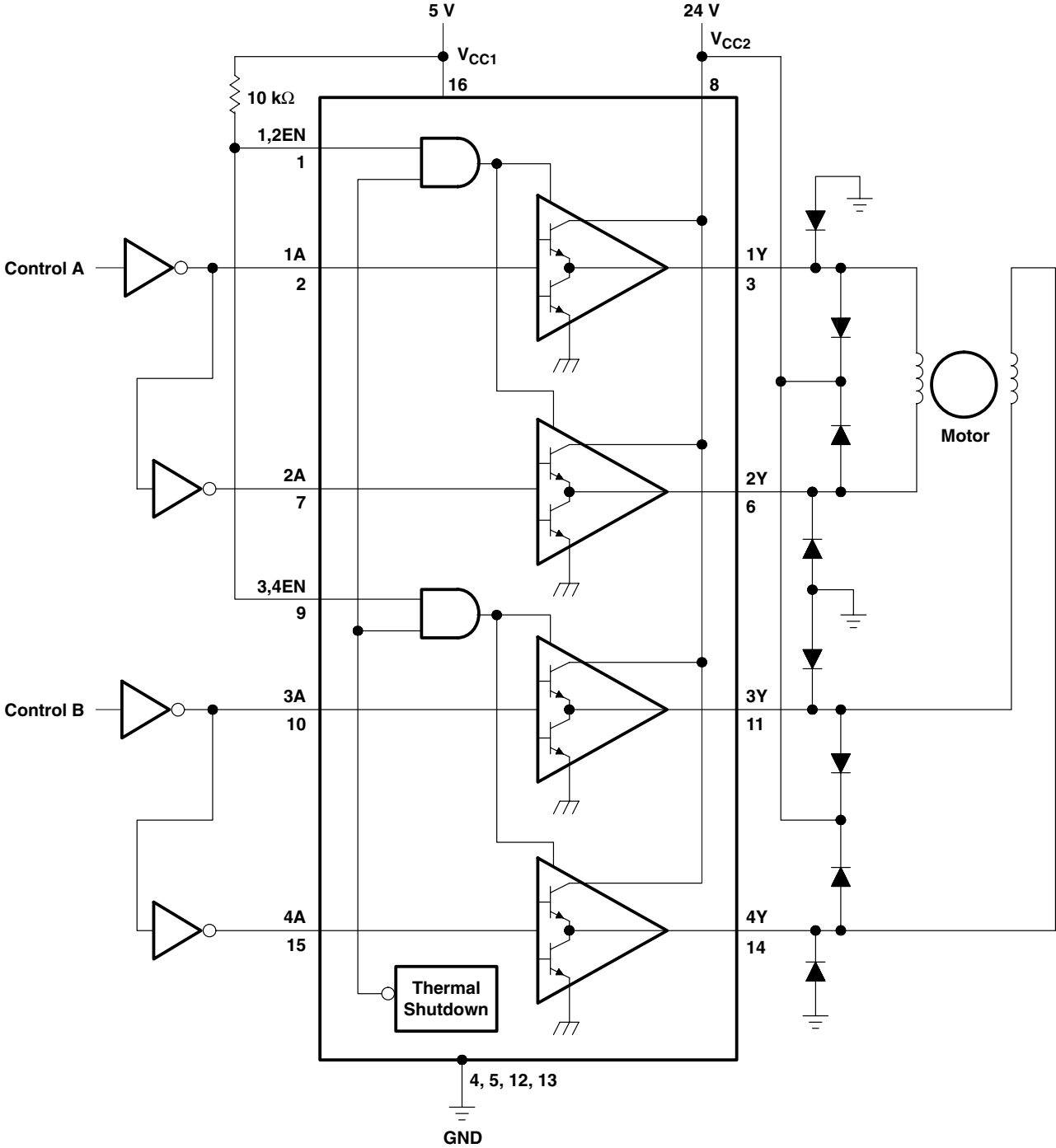


Figure 2. Two-Phase Motor Driver (L293)

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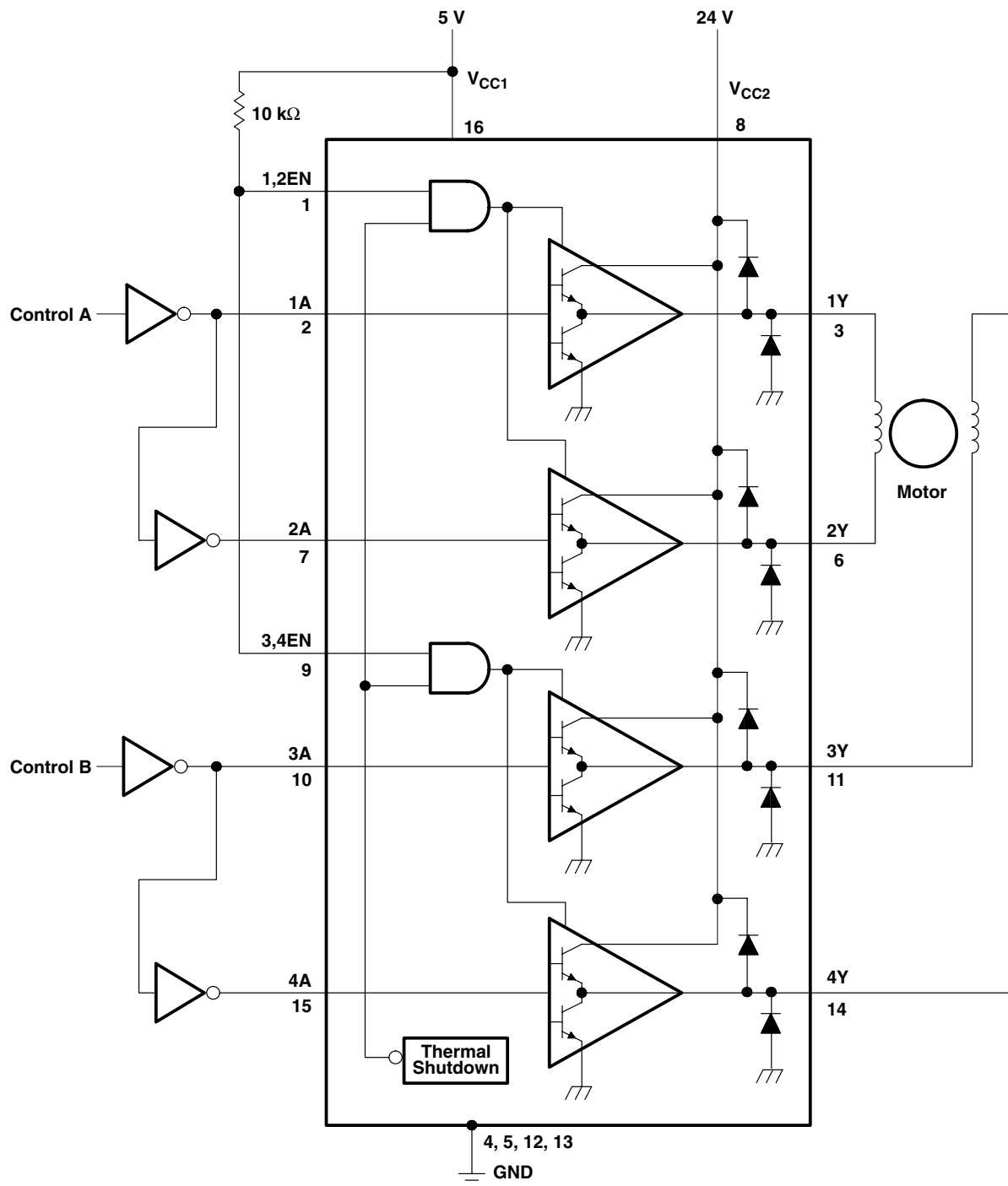
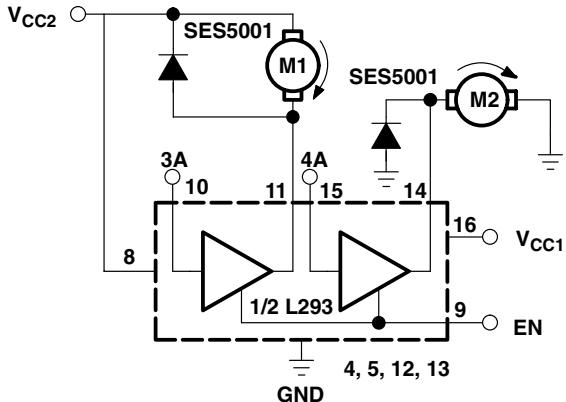


Figure 3. Two-Phase Motor Driver (L293D)

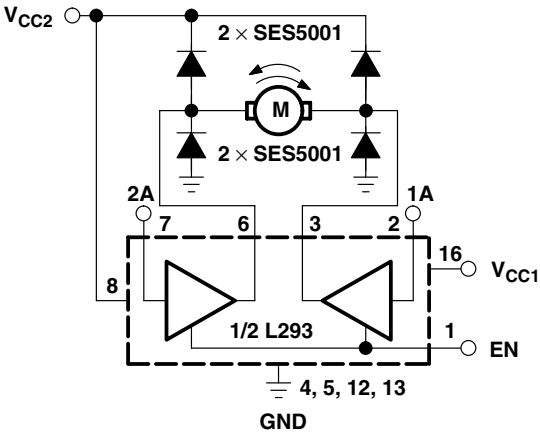
APPLICATION INFORMATION



| EN | 3A | M1 | 4A | M2 |
|----|----|-------------------------|----|-------------------------|
| H | H | Fast motor stop | H | Run |
| H | L | Run | L | Fast motor stop |
| L | X | Free-running motor stop | X | Free-running motor stop |

L = low, H = high, X = don't care

**Figure 4. DC Motor Controls
(connections to ground and to supply voltage)**



| EN | 1A | 2A | FUNCTION |
|----|----|----|-----------------|
| H | L | H | Turn right |
| H | H | L | Turn left |
| H | L | L | Fast motor stop |
| H | H | H | Fast motor stop |
| L | X | X | Fast motor stop |

L = low, H = high, X = don't care

Figure 5. Bidirectional DC Motor Control

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APPLICATION INFORMATION

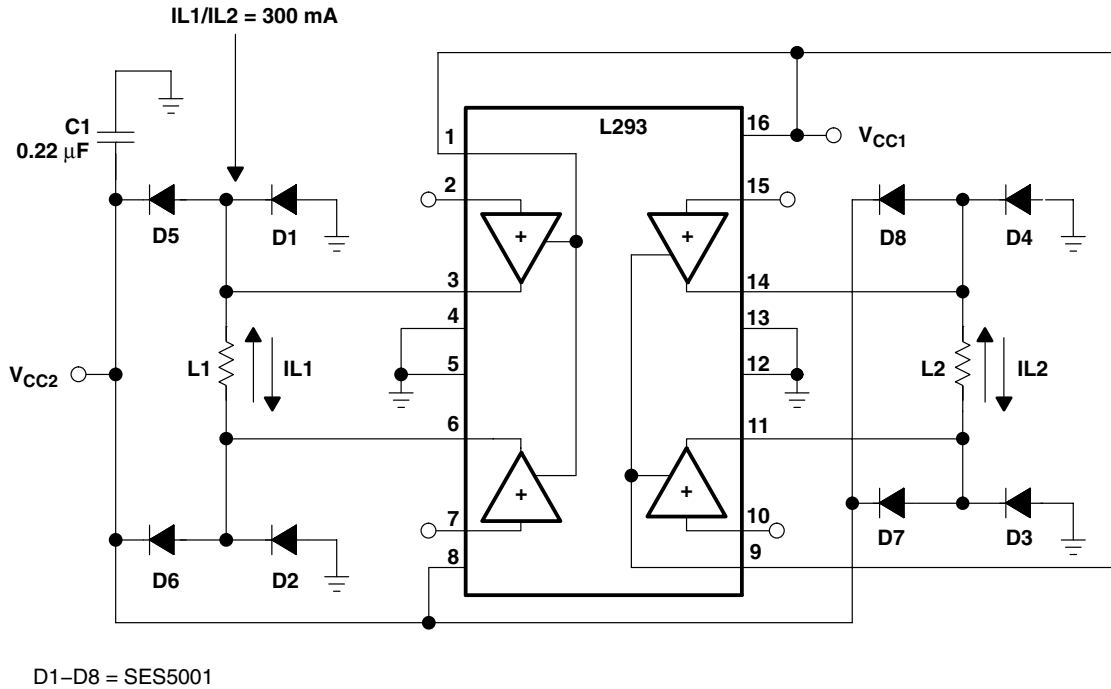


Figure 6. Bipolar Stepping-Motor Control

mounting instructions

The $R_{th(j-c)}$ of the L293 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board or to an external heat sink.

Figure 9 shows the maximum package power P_{TOT} and the θ_{JA} as a function of the side l of two equal square copper areas having a thickness of 35 μ m (see Figure 7). In addition, an external heat sink can be used (see Figure 8).

During soldering, the pin temperature must not exceed 260°C, and the soldering time must not exceed 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

APPLICATION INFORMATION

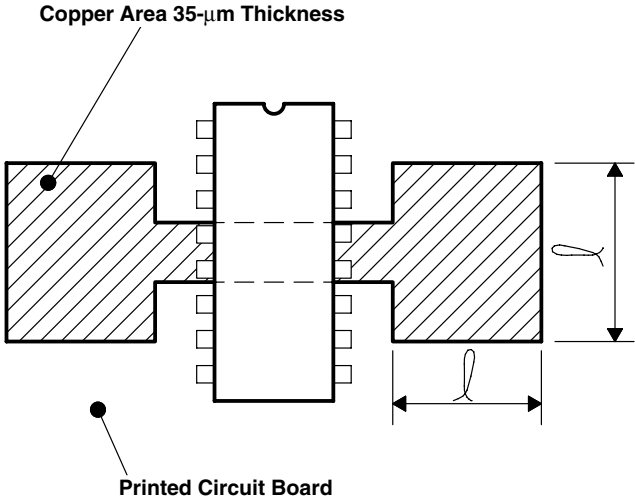


Figure 7. Example of Printed Circuit Board Copper Area (used as heat sink)

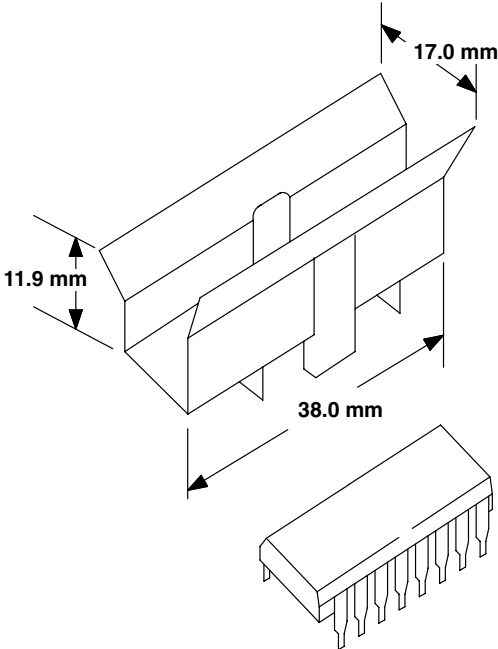


Figure 8. External Heat Sink Mounting Example ($\theta_{JA} = 25^{\circ}\text{C/W}$)

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APPLICATION INFORMATION

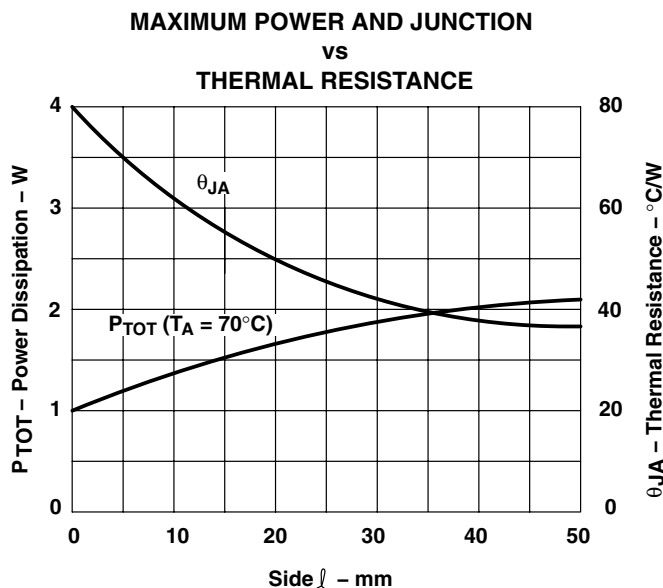


Figure 9

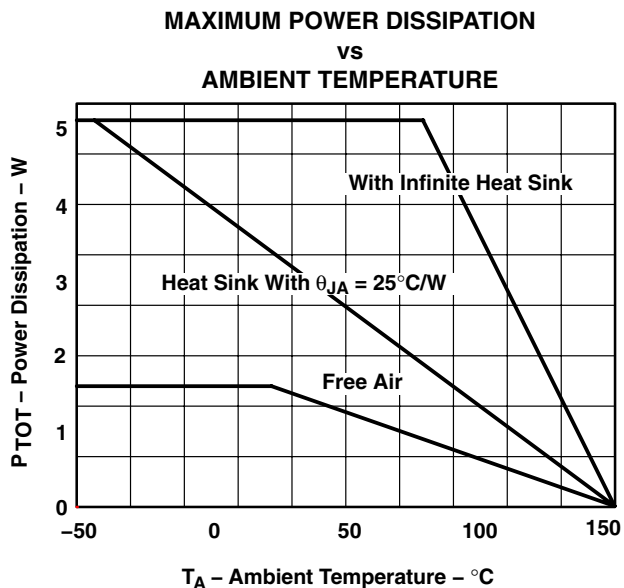


Figure 10

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|-------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| L293DNE | ACTIVE | PDIP | NE | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | L293DNE | Samples |
| L293DNEE4 | ACTIVE | PDIP | NE | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | L293DNE | Samples |
| L293DWP | OBSOLETE | SOIC | DW | 28 | | TBD | Call TI | Call TI | 0 to 70 | L293DWP | |
| L293DWPG4 | OBSOLETE | SOIC | DW | 28 | | TBD | Call TI | Call TI | 0 to 70 | | |
| L293DWPTR | OBSOLETE | SO PowerPAD | DWP | 28 | | TBD | Call TI | Call TI | 0 to 70 | | |
| L293N | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI | 0 to 70 | L293N | |
| L293NE | ACTIVE | PDIP | NE | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | L293NE | Samples |
| L293NEE4 | ACTIVE | PDIP | NE | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | L293NE | Samples |
| L293NG4 | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI | 0 to 70 | | |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

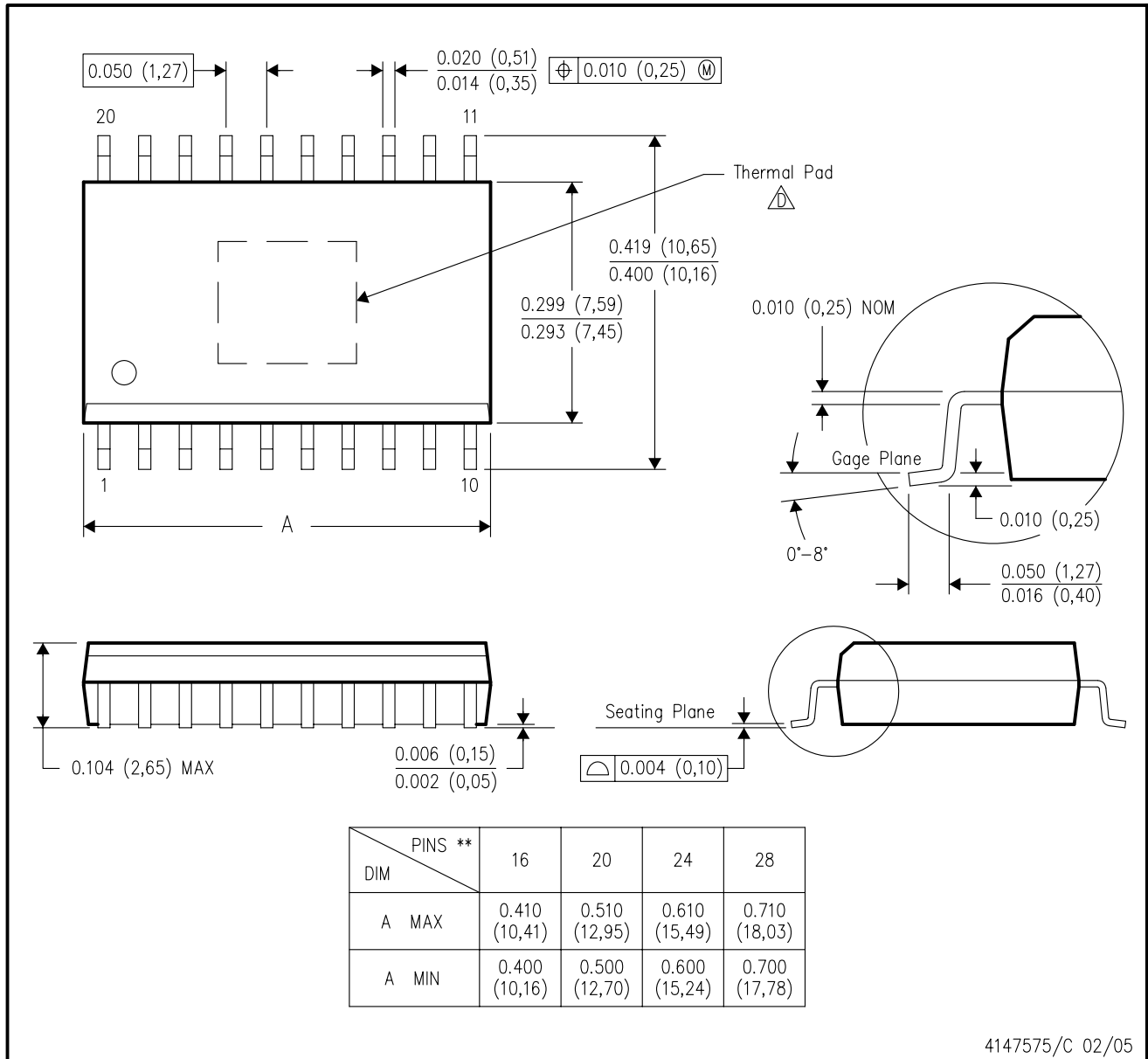
⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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DWP (R-PDSO-G**) 20 PINS SHOWN

PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE

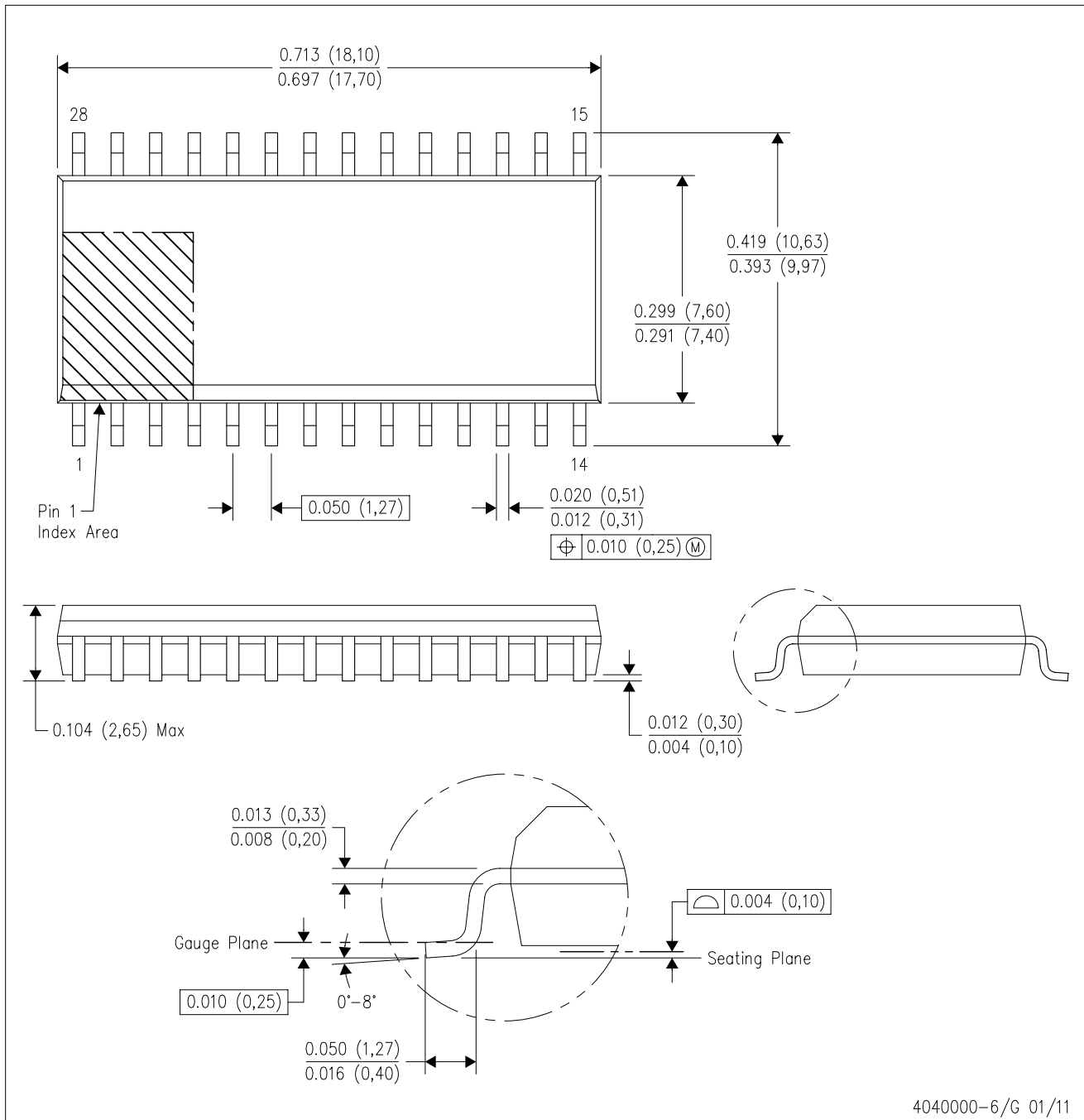


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>. See the product data sheet for details regarding the exposed thermal pad dimensions.

PowerPAD is a trademark of Texas Instruments.

DW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



4040000-6/G 01/11

- NOTES:
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 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AE.

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